CLAIMS

What is claimed is:

1. An apparatus for preventing buffers used to reduce delays on relatively long conductive signal lines of an IC from being damaged during manufacturing of the IC, the apparatus comprising:

a buffer having an input connected to one of said conductive signal lines of an IC that comprises the buffer;

a protection diode comprised by said buffer, the protection diode being coupled to the input of the buffer, the protection diode pulling at least some electrical charge off of one or more transistor gates of one or more respective transistors of the buffer to prevent the buffer from being damaged by too much electrical charge collecting on one or more transistor gates of respective transistors of the buffer.

2. The apparatus of claim 1, wherein every buffer of the IC comprises a protection diode.

3. The apparatus of claim 1, wherein only buffers of the IC that have been determined to need protection diodes comprise a protection diode.

4. The apparatus of claim 1, wherein the size of the protection diode in terms of area is at least partially dependent on the gate area of at least one of the transistor gates of the buffer that is available for storing electrical charge.

5. The apparatus of claim 1, wherein each buffer comprises two inverters, each inverter comprising at least one P field effect transistor (PFET) and at least one N field effect transistors (PFET), each PFET and each NFET having a gate a source and a drain, and wherein electrical charge collects on the gates of at least the PFET and NFET of at least one of the inverters.

6. The apparatus of claim 1, wherein each buffer comprises two inverters that utilize bipolar junction transistor (BJT) technology.

7. The apparatus of claim 1, wherein the size of the protection diode in terms of area is at least partially dependent on dimensions of the conductive signal line to which the buffer input is connected.

8. The apparatus of claim 1, wherein the size of the protection diode in terms of area is dependent on dimensions of the conductive signal line to which the buffer input is connected and on the gate area of at least one of the transistor gates of the buffer that is available for storing electrical charge.

9. The apparatus of claim 1, wherein the size for the protection diode in terms of area depends at least partially on the IC process used to design the IC.

10. A method for preventing buffers used to reduce delays on relatively long conductive signal lines of an IC from being damaged due to electrical charges that collect on the buffers during manufacturing of the IC, the method comprising the steps of:

buffering one of said relatively long conductive signal lines of an IC with a buffer to reduce delays in said one of said relatively long conductive signal lines, said buffer comprising a protection diode, the protection diode being coupled to an input of the buffer, the protection diode pulling at least some of the electrical charge off of one or more transistor gates of one or more respective transistors of the buffer to prevent the buffer from being damaged by too much electrical charge collecting on one or more transistor gates of respective transistors of the buffer.

11. The method of claim 10, wherein every buffer of the IC comprises a protection diode.

12. The method of claim 10, further comprising the step of determining whether a buffer needs a protection diode before including a protection diode in the buffer, wherein only buffers of the IC that have been determined to need protection diodes comprise a protection diode.

13. The method of claim 10, wherein the size of the protection diode in terms of area is at least partially dependent on the gate area of at least one of the transistor gates of the buffer that is available for storing electrical charge.

14. The method of claim 10, wherein the size of the protection diode in terms of area is preselected.

15. The method of claim 10, wherein the IC is manufactured using bipolar junction transistor process technology.

16. The method of claim 10, wherein the IC is manufactured using filed effect transistor process technology.

17. The method of claim 10, wherein the size of the protection diode in terms of area is at least partially dependent on dimensions of the conductive signal line to which the buffer input is connected.

18. The method of claim 10, wherein the size of the protection diode in terms of area is dependent on dimensions of the conductive signal line to which the buffer input is connected and on the gate area of at least one of the transistor gates of the buffer that is available for storing electrical charge.

19. The method of claim 10, wherein the size for the protection diode in terms of area depends at least partially on the IC process used to design the IC.

20. The method of claim 11, wherein the size for the protection diode in terms of area is preselected.